

Form PTO-1449 (Modified)
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ATTY. DOCKET NO.

SERIAL NO.

254-094-CIP4/CIP-MB

10/828,495

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

APPLICANT

Julian Partridge & James D. Wehrly, Jr.

FILING DATE

4/20/2004

GROUP

2822

(37 CFR 1.98(b))

U.S. PATENT DOCUMENTS

*Examiner Initial	Patent Number		Patentee	Class	Subclass	Filing Date (if appropriate)
TYT	5,428,190	6/27/1995	Stopperan	174/261		7/2/1993
	6,097,087	8/1/2000	Farnworth, Warren M. et al	257/698		10/31/1997
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	6,351,029B1	2/26/2002	Isaak	257/688		5/19/2000
	6,368,896B2	4/9/2002	Farnworth, Warren M. et al	438/113		4/23/1999
	6,410,857B1	6/25/2002	Gonya	174/254		8/13/2001
	6,426,240B2	7/30/2002	Isaak	438/106		6/25/2001
	6,426,549B1	7/30/2002	Isaak, Harlan R.	257/686		11/3/2000
	6,444,921B1	9/3/2002	Wang, et al	174/260		2/3/2000
	6,465,877B1	10/15/2002	Farnworth, Warren M. et al	257/668		3/27/2000
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FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
TYT	58-96756(A)	06/08/1983	Japan			Partial	
	58-112348(A)	07/04/1983	Japan			Partial	
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TYT	Dense-Pac Microsystems, Breaking Space Barriers, 3-D Technology 1993
	Dense-Pac Microsystems, DPS512X16A3, Ceramic 512K X 16 CMOS SRAM Module
	"Design Techniques for Ball Grid Arrays," William R. Newberry, Xynetix Design Systems, Inc.

EXAMINER

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U.S. PATENT DOCUMENTS

*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
TYT	6,262,895 B1	7/17/2001	Forthum, John A.	361/749		1/13/2000
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	6,028,365	2/22/2000	Akram et al.	257/778		3/30/1998
	6,433,418	8/13/2002	Fujisawa et al.	257/696		4/29/1999
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	6,265,660 B1	7/24/2001	Tandy, Patrick W.	174/52.4		8/18/2000
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	6,462,412 B2	10/8/2002	Kamei et al	257/723		1/17/2001
	6,465,893 B1	10/15/2002	Khandros et al.	257/777		10/19/2000
	6,486,544 B1	11/26/2002	Hashimoto, Nobuaki	257/686		9/3/1999
	6,560,117 B2	5/6/2003	Moon, Ow Chee	361/749		8/30/2001
	6,590,282 B1	7/8/2003	Wang et al.	257/686		4/12/2002
	6,600,222 B1	7/29/2003	Levarado, Melvin N.	257/686		7/17/2002

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						Yes	No
TYT	62-230027(A)	10/08/1987	Japan			Partial	

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TYT	"Chip Scale Packaging and Redistribution," Paul A. Magill, Glenn A. Rinne, J. Daniel Mis, Wayne C. Machon, Joseph W. Baggs, Unitive Electronics Inc.
TYT	"3D Interconnection for Ultra-Dense Multichip Modules," Christian VAL, Thomson-CSF DCS Computer Division, Thierry Lemoine, Thomson-CSF RCM Radar Countermeasures Division
	"High Density Memory Packaging Technology High Speed Imaging Applications," Dean Frew, Texas Instruments Incorporated
	Teresa Technologies, Inc. - Semiconductor Intellectual Property, Chip Scale Packaging - Website pages (3)

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TYT	6,620,651B2	9/16/2003	He et al.	438/113		10/23/2001
	US2002/0139577A1	10/3/2002	Miller, Charles A.	174/261		3/27/2001
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	4,823,234	04/18/1989	Konishi, et al	361/386		07/01/1986
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Document Number	Date	Country	Class	Subclass	Translation	
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TYT	"Tessera Introduces uZ™ - Ball Stacked Memory Package for Computing and Portable Electronic Products" Joyce Smaragdis, Tessera Public Relations; 2 figures that purport to be directed to the uZ™ - Ball Stacked Memory Package.
TYT	Ron Bauer, Intel. "Stacked-CSP Delivers Flexibility, Reliability, and Space-Saving Capabilities", Spring 2002.
TYT	Tessera uZ Ball Stack Package. 4 figures that purport to be directed to the uZ - Ball Stacked Memory. 1 Page.
TYT	"Vertically-Integrated Package," Alvin Weinberg, Pacesetter, Inc. and W. Kinzy Jones, Florida International University

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GROUP 2222

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*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
TNT	4,983,533	01/08/1991	Go	437/7		10/28/1987
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	5,099,393	03/24/1992	Bentlage, et al	361/413		03/25/1991
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	5,159,434	10/27/1992	Kohno, et al	357/80		02/01/1991
	5,222,014	06/22/1993	Lin	361/414		03/02/1992
	5,224,023	06/29/1993	Smith, et al.	361/412		02/10/1992
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	5,949,657	09/07/1999	Karabatsos	361/803		08/25/1998
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